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TITLE: Generating arbitrarily phase shifted digital
signal - dividing frequency of original signal and
supplying to two variable phase shifters

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Basic Abstract Text - ABTX (1):

The HF clock pulse signal has its phase shifted by an arbitrarily adjustable phase value between zero and π , using adjustable phase shifters between zero and $\pi/2$ or $3\pi/4$. The original signal (T) frequency is divided and phase shifted of the divided signal from $0-\pi/2$ and π are generated. The process uses two variable phase shifters such that the first one input is supplied with a non-delayed, or with a $-\pi/2$ phase shifted, frequency divided signal.

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	50239	system near2 clock	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 07:25
L2	186	arbitrar\$4 near5 ((adjust\$4 correcting forc\$4) near3 phase)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 08:14
L3	10	1 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 07:27
L4	24	2 same clock	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 07:43
L5	19	4 not 3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 08:09
L6	0	zero adj forfing	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 08:09
L7	911	zero adj forcing	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 08:12
L8	0	7 near3 (phase near2 clock)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 08:10
L9	6	7 near3 phase	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 08:12
L10	105	arbitrar\$4 same ((adjust\$4 correcting forc\$4) near3 phase) same clock	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 10:26
L11	9	master same 10	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 08:45
L12	98	zero adj phase adj detector	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 08:46

L13	6	12 near4 clock	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 08:57
L14	27090	phase near2 delay	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 08:57
L15	11909	master adj clock	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 08:57
L16	126	14 same 15	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 08:58
L17	11	1 same 16	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 09:05
L18	291	14 same 1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 09:05
L19	9723	arbitrar\$4 near3 ((adjust\$4 correct\$4))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 09:07
L20	0	18 same 19	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 09:30
L21	0	18 same 19	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 10:07
L22	13521	cfm (clock adj2 master)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 10:08
L23	20194	output adj driver	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 10:08
L24	13	22 same 23	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 10:08

L25	162	arbitrar\$4 same ((adjust\$4 correct\$4 forc\$4) near3 phase) same clock	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 10:27
L26	12	master same 25	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 10:27
L27	3	26 not 11	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/25 10:27